TRACKS

- FPGA (₹ 20,000)
- RASPBERRY PI / RENESAS KIT (₹ 15,000)
- ESP/ARDUINO (₹ 10,000)

PRIZE POOL UP TO ₹ 45,000

Eligibility:

- **B.Tech/ M.Tech/ PhD students**
- **Team Size: 3–5 members.**
- **Members must be from the same institute**
- **A team may contain members of any degree**

KEY FOCUS AREAS

01 **Hardware-Centric Innovation**
FPGA, Raspberry Pi & Microcontroller-based solutions.

02 **Optimized Hardware Design**
Low power, low latency, and efficient resource utilization.

03 **Real-Time Performance**
Fast, reliable, and scalable hardware implementation.

04 **Edge AI & Embedded Systems**
Intelligent on-device computing with real-time processing.

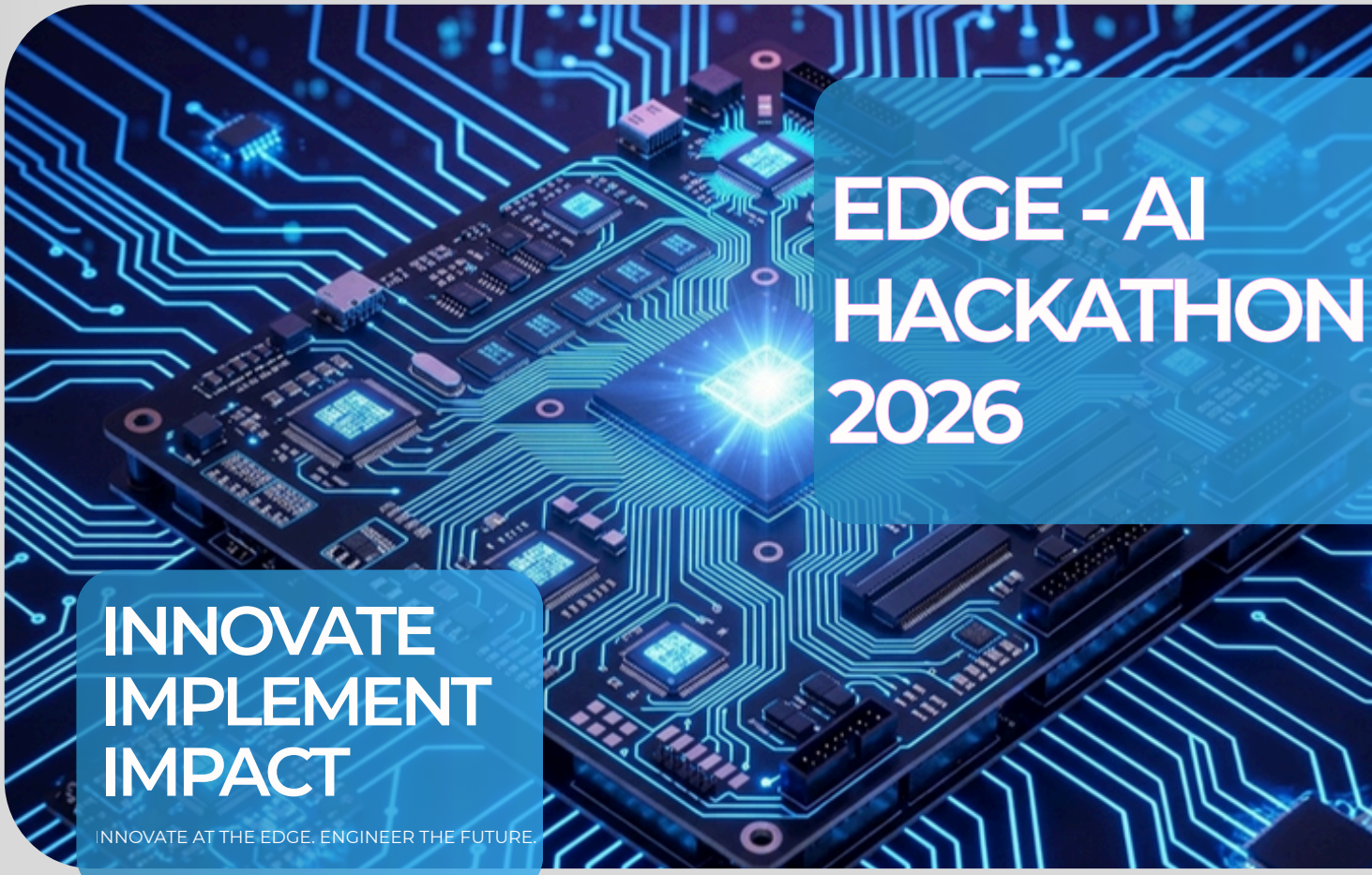
CEDA® IEEE Council on Electronic Design Automation

IEEE Advancing Technology for Humanity

BPUT, ODISHA ESTD-2009

Electron Devices Society

Chips to Startup Programme



EDGE - AI HACKATHON 2026

INNOVATE IMPLEMENT IMPACT

INNOVATE AT THE EDGE. ENGINEER THE FUTURE.

TIME LINE

Round 0 (Abstract Submission)
AUGUST 15, 2026

Round 0 (Result Announcement)
SEPTEMBER 18 ,2026

Round 1 (Software Simulation)
SEPTEMBER 18 - OCTOBER 04, 2026

Round 2 (Hardware Implementation)
OCTOBER 04 - OCTOBER 06, 2026 (On site)

ORGANISATION & SPONSORSHIP

IEEE CEDA & EDS STUDENT CHAPTER,
IEEE STUDENT BRANCH, PMEC

IEEE BHUBANESWAR SECTION

TECHNICAL SPONSOR

AMD RENESAS ETiOS MICROCHIP

Parala Maharaja Engineering College, Brahmapur

ABOUT PARALA MAHARAJA ENGINEERING COLLEGE, ODISHA

Parala Maharaja Engineering College (PMEC), Berhampur, established on 26 April 2009, is the only Government Engineering College in South Odisha. Autonomous since 2021 and affiliated with BPUT, Odisha, the institute offers 8 B.Tech, 7 M.Tech, and Ph.D. research programmes. Spread across an 80-acre campus with modern academic infrastructure, advanced laboratories, a central library, workshops, hostels, and research facilities, PMEC is committed to excellence in technical education, innovation, and the production of industry-ready engineers. Located in the historic Silk City of Berhampur, Odisha, the institute provides an ideal environment for learning, research, and technological advancement.

ABOUT ELECTRONICS AND TELECOMMUNICATION DEPARTMENT

Established in 2013, the Department of Electronics & Telecommunication Engineering offers quality education in Communication Systems, VLSI Design, Embedded Systems, Image & Signal Processing, and Edge AI. The department provides hands-on learning through state-of-the-art laboratories equipped with FPGA development boards, Renesas kits, industry-standard EDA tools, and advanced communication laboratories, preparing students for careers in both core electronics and IT industries.

ABOUT IEEE STUDENT BRANCH CHAPTERS

IEEE Student Branch PMEC

Established in 2024, the IEEE Student Branch at PMEC is among the fastest-growing IEEE student communities in Odisha. It promotes technical excellence through workshops, competitions, industry interaction, and research-driven activities.

- Established: November 2024
- Members: 80+ Student Members
- Recognition: Odisha's 2nd Largest IEEE Student Branch

IEEE Council on Electronic Design Automation (CEDA) & Electron Devices Society (EDS) PMEC SBC

The IEEE CEDA Student Branch Chapter promotes Electronic Design Automation (EDA), FPGA, ASIC, and SoC design, supporting students in developing next-generation hardware solutions while strengthening the C2S ecosystem at PMEC.

The IEEE EDS Student Branch Chapter, established in 2026, focuses on semiconductor devices, VLSI, embedded systems, Edge AI, and hardware innovation by organizing technical talks, workshops, hackathons, and collaborative research initiatives.

- Established: April 2026
- Members: 44+ Student Members
- Focus: Semiconductor Devices, VLSI, Embedded Systems & Edge AI

C2S@PMEC

PMEC is a proud participant in the Chips to Startup (C2S) Programme by MeitY, Government of India, supported by a ₹65.19 lakh grant. The initiative has established advanced laboratories with FPGA platforms, ASIC design flow, and industry-standard EDA tools. As a key achievement, PMEC successfully designed and fabricated IC-C2S0061, an indigenous multiplier IC, through SCL Chandigarh, showcasing the institute's growing expertise in semiconductor and VLSI design.

ABOUT EDGE AI HACKATHON 2026

Edge AI Hackathon 2026 is a national-level hardware innovation challenge organized by the IEEE EDS Student Branch Chapter, PMEC, encouraging participants to design and implement real-time Edge AI solutions on FPGA, Raspberry Pi, Renesas, and Microcontroller platforms. The hackathon bridges innovation, embedded intelligence, and hardware acceleration to solve real-world engineering challenges.

PROBLEM DOMAINS

Communication Systems

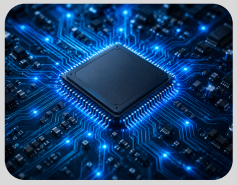
Design intelligent and efficient solutions for wireless communication, networking, signal transmission, and IoT connectivity.

Biomedical Engineering

Develop embedded systems for healthcare applications, including patient monitoring, medical imaging, and wearable devices.

Image & Signal Processing

Implement real-time algorithms for image enhancement, object detection, audio analysis, and sensor data processing.



Processors

Develop optimized processor architectures, digital systems, and embedded hardware with a focus on performance, power efficiency, and real-time execution.

Defence & Security

Build reliable hardware solutions for secure communication, surveillance, navigation, and threat detection.

Indian Knowledge System

Develop AI-powered solutions for preserving, enhancing, and delivering valuable knowledge through intelligent digital platforms and embedded systems.

DETAILS OF THE EVENT

ROUND 0 (ONLINE)

Teams must submit an abstract outlining their proposed solution, innovation, methodology, workflow, expected outcomes, and the hardware/software tools to be used. Submissions will be evaluated for innovation, technical feasibility, implementation approach, and real-world impact. The abstract submission link is available in the Linktree.

ROUND 1 (ONLINE)

Teams will develop and validate their proposed solution using appropriate software tools such as Vivado, MATLAB, Python, C/C++, or simulation platforms. Round 1 will be conducted in online mode.

ROUND 2 (ON-SITE)

DAY- 01

Qualified teams will implement their solutions on the designated hardware platform (FPGA, Raspberry Pi, or Microcontroller) and demonstrate real-time functionality. Mentors and judges will evaluate hardware design, system optimization, and overall performance.

DAY- 02

Teams will present their complete solution through a live demonstration and technical presentation, followed by a Q&A session with the judging panel. Winners will be selected based on innovation, technical excellence, hardware implementation, and real-world impact, followed by the prize distribution ceremony.

EVALUATION CRITERIA

Innovation & Technical Excellence – Originality, creativity, and technical depth of the solution.
Implementation & Performance – Functionality, design quality, feasibility, and execution of the prototype.
Presentation & Impact –
Clarity of presentation, demonstration, scalability, and real-world applicability.

Team Details & Registration :

Team Size:

- **Minimum: 3, Maximum: 5 members per team.**

Registration Fee:

- **₹1200 per participant. (₹1000 for IEEE members) This fee includes food and registration kit charges.**
- **Hostel accommodation is available free of cost.**
- **No TA/DA will be provided.**

Registration:

RULES & GUIDELINES

- All project ideas, designs, and implementations must be original. Plagiarism or copied work will result in immediate disqualification.
- Each team must select one problem statement from the official list (6 domains × 6 problem statements) available via the Linktree.
- Round 0 (Abstract Submission) is mandatory. Abstracts must be submitted only in the prescribed template provided in the Linktree.
- Teams must submit their registration and abstract via the respective links on the Linktree.
- Development boards (FPGA, Renesas Kit, Raspberry Pi, ESP32, Arduino, etc) will be provided by the organisers. The list of supported boards will be shared in advance.
- Teams must bring their own sensors, actuators, modules, and other required peripherals for project implementation.
- The decision of the judges and organising committee shall be final and binding.

AVAILABLE BOARDS FOR DEVELOPMENT

Available Development Boards :

- PYNQ-Z2
- Basys 3
- Arty A7-100T
- Kria KR260
- Kria KV260 (Vision AI Starter Kit)
- Zynq UltraScale+ MPSoC ZCU104
- Raspberry Pi 5
- Raspberry Pi I/O Board
- Urbana Board
- Boolean Board
- Renesas QuickConnect Beginners Kit V2.0
- Renesas EK-RA6M5 Evaluation Kit
- Renesas EK-RA8D1 Evaluation Kit
- ESP32

Available PMOD Modules :

- PMOD KYPD (16-Button Keypad)
- PMOD OLEDRGB (96 × 64 RGB OLED Display)
- PMOD DA2 (Dual 12-bit DAC)
- PMOD TPH2 (12-Pin Test Point Header)

LINK TREE

ABSTRACT FORMAT

EDGE-AI_ABSTRACT_FORMAT

ABSTRACT SUBMISSION & REGISTRATION FORM

GOOGLE FORM

PROBLEM STATEMENTS

PROBLEM STATEMENT LINK

WEBSITE FOR MORE INFORMATION

WEBSITE

CONTACT INFO

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